AMENDMENTS IN THE CLAIMS:

1. (Original) A nitride-based semiconductor device comprising: a substrate structure with electrical conductivity; and a semiconductor multilayer structure that is supported on the substrate structure,

wherein the principal surface of the substrate structure has at least one vertical growth region, which functions as a seed crystal for growing a nitride-based semiconductor vertically, and a plurality of lateral growth regions for allowing the nitride-based semiconductor that has grown on the vertical growth region to grow laterally, and

wherein the sum ΣX of the respective sizes of the vertical growth regions as measured in a first direction, which is parallel to the principal surface of the substrate structure, and the sum ΣY of the respective sizes of the lateral growth regions as measured in the first direction satisfy the inequality $\Sigma X/\Sigma Y > 1.0$.

2. (Original) The nitride-based semiconductor device of claim 1, wherein the substrate structure is made of $Al_{x1}Ga_{y1}In_{z1}N$ crystals (where $x1+y1+z1=1$, $x1 \geq 0$, $y1 \geq 0$ and $z1 \geq 0$), and

wherein the semiconductor multilayer structure includes an $Al_{x2}Ga_{y2}In_{z2}N$ crystal layer (where $x2+y2+z2=1$, $x2 \geq 0$, $y2 \geq 0$ and $z2 \geq 0$) that has grown from the vertical growth region on the principal surface of the substrate structure.

3. (Original) The nitride-based semiconductor device of claim 1, wherein the substrate structure includes:

a substrate body made of $Al_{x1}Ga_{y1}In_{z1}N$ crystals (where $x1+y1+z1=1$, $x1\geq0$, $y1\geq0$ and $z1\geq0$); and

an $Al_{x3}Ga_{y3}In_{z3}N$ crystal layer (where $x3+y3+z3=1$, $x3\geq0$, $y3\geq0$ and $z3\geq0$), which has been formed on the upper surface of the substrate body and of which the surface functions as the principal surface of the substrate structure, and

wherein the semiconductor multilayer structure includes an $Al_{x2}Ga_{y2}In_{z2}N$ crystal layer (where $x2+y2+z2=1$, $x2\geq0$, $y2\geq0$ and $z2\geq0$) that has grown from the vertical growth region on the principal surface of the substrate structure.

4. (Original) The nitride-based semiconductor device of claim 1, wherein the vertical and lateral growth regions on the principal surface of the substrate structure extend in stripes perpendicularly to the first direction.

5. (Original) The nitride-based semiconductor device of claim 4, wherein the vertical growth region on the principal surface of the substrate structure is defined by a striped ridge portion that is present on the principal surface of the substrate structure.

6. (Currently Amended) The nitride-based semiconductor device of claim 4 ~~or 5~~, further comprising a mask layer that covers the principal surface of the substrate structure,

wherein the mask layer includes a striped opening, which is aligned with the vertical growth region, and masking portions, which are aligned with the lateral growth regions.

7. (Original) The nitride-based semiconductor device of claim 6, wherein the area of the opening of the mask layer is greater than the overall area of the masking portions of the mask layer.

8. (Original) The nitride-based semiconductor device of claim 2, wherein the semiconductor multilayer structure includes an active layer, of which the bandgap is smaller than that of the $Al_{x2}Ga_{y2}In_{z2}N$ crystal layer, and

wherein the device further includes a current confining structure for injecting carriers into a part of the active layer.

9. (Original) The nitride-based semiconductor device of claim 8, wherein the current confining structure is located right over the lateral growth regions on the principal surface of the substrate structure.

10. (Original) The nitride-based semiconductor device of claim 3, wherein the $Al_{x3}Ga_{y3}In_{z3}N$ layer has a structure in which at least one of the mole fractions x3, y3 and z3 of its constituents changes in the thickness direction thereof.

11. (Original) The nitride-based semiconductor device of claim 10, wherein the $Al_{x3}Ga_{y3}In_{z3}N$ layer includes at least two layers.

12. (Original) A method for fabricating a nitride-based semiconductor device, the method comprising the steps of:

(A) providing a substrate structure, which has, on its principal surface, a plurality of vertical growth regions functioning as a seed crystal for growing a nitride-based semiconductor vertically and a plurality of lateral growth regions for allowing the nitride-based semiconductor that has grown on the vertical growth regions to grow laterally, the substrate structure satisfying the inequality $X/Y>1.0$, where X is the size of each said vertical growth region as measured in a first direction, which is parallel to the principal surface of the substrate structure, and Y is the size of each said lateral growth region as measured in the first direction; and

(B) growing a nitride-based semiconductor layer on the principal surface of the substrate structure.

13. (Original) The method of claim 12, wherein the step (A) includes the step of providing a wafer made of $Al_{x1}Ga_{y1}In_{z1}N$ crystals (where $x1+y1+z1=1$, $x1\geq0$, $y1\geq0$ and $z1\geq0$) as the substrate structure, and

wherein the step (B) includes the step of growing an $Al_{x2}Ga_{y2}In_{z2}N$ crystal layer (where $x2+y2+z2=1$, $x2\geq0$, $y2\geq0$ and $z2\geq0$), functioning as the nitride-based semiconductor layer, from the vertical growth regions on the principal surface of the substrate structure.

14. (Original) The method of claim 12, wherein the step (A) includes the steps of:

(a1) providing a wafer made of $Al_{x1}Ga_{y1}In_{z1}N$ crystals (where $x1+y1+z1=1$, $x1\geq0$, $y1\geq0$ and $z1\geq0$) as a substrate body; and

(a2) growing an $Al_{x3}Ga_{y3}In_{z3}N$ crystal layer (where $x3+y3+z3=1$, $x3\geq0$, $y3\geq0$ and $z3\geq0$), of which the surface functions as the principal surface of the substrate structure, on

the upper surface of the substrate body, and

wherein the step (B) includes growing an $Al_{x2}Ga_{y2}In_{z2}N$ crystal layer (where $x2+y2+z2=1$, $x2 \geq 0$, $y2 \geq 0$ and $z2 \geq 0$), functioning as the nitride-based semiconductor layer, from the vertical growth regions on the principal surface of the substrate structure.

15. (Original) The method of claim 12, wherein the vertical and lateral growth regions on the principal surface of the substrate structure extend in stripes perpendicularly to the first direction.

16. (Original) The method of claim 15, wherein the vertical growth regions on the principal surface of the substrate structure are defined by striped ridge portions that are present on the principal surface of the substrate structure.

17. (Original) The method of claim 16, wherein the step (A) includes the steps of:

covering the principal surface of the substrate structure with a resist mask that has a pattern defining the vertical growth regions; and

selectively etching away exposed portions of the principal surface of the substrate structure that are not covered with the resist mask.

18. (Currently Amended) The method of claim 16 ~~or 17~~, wherein the device further includes a mask layer that covers the principal surface of the substrate structure, and

wherein the mask layer includes striped openings, which are aligned with the vertical growth regions, and masking portions, which are aligned with the lateral growth regions.

19. (Original) The method of claim 18, wherein the overall area of the openings of the mask layer is greater than that of the masking portions of the mask layer.

20. (Currently Amended) The method of claim 13 ~~or 14~~, further comprising the step (C) of forming a semiconductor multilayer structure including the nitride-based semiconductor layer and other semiconductor layers that have been stacked on the nitride-based semiconductor layer,

wherein the step (C) includes the steps of

(c1) forming an active layer, of which the bandgap is smaller than that of the $Al_{x2}Ga_{y2}In_{z2}N$ crystal layer, and

(c2) forming a current confining structure for injecting carriers into a part of the active layer.

21. (Original) The method of claim 20, wherein the step (c2) includes the step of arranging the current confining structure right over the lateral growth regions on the principal surface of the substrate structure.

22. (Original)The method of claim 15, wherein the step (a2) includes the step of changing at least one of the mole fractions x3, y3 and z3 of the constituents of the $Al_{x3}Ga_{y3}In_{z3}N$ layer in the thickness direction thereof.

23. (Original) The method of claim 22, wherein the $Al_{x3}Ga_{y3}In_{z3}N$ layer includes at least two layers.

24. (Original) The method of claim 13, wherein the step (a2) includes the step of changing growth temperatures while the $Al_{x3}Ga_{y3}In_{z3}N$ layer is growing.

25. (Original) The method of claim 12, wherein at least one of X and Y changes from one position to another on the principal surface of the substrate structure as a wafer.